COURSE DESCRIPTION CARD - SYLLABUS

Course name
Digital logic design [S1MiKC2>ProjUC]

Course

Field of study
Microelectronics and Digital Communication

Year/Semester
2/4

Area of study (specialization)
–

Profile of study
general academic

Level of study
first-cycle

Course offered in
Polish

Form of study
full-time

Requirements
compulsory

Number of hours

Lecture
15

Laboratory classes
30

Other
0

Tutorials
0

Projects/seminars
0

Number of credit points

2,00

Coordinators

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Lecturers

Prerequisites

Ability to analyze and design simple digital, combinational and sequential, circuits and devices. A basic knowledge of Boolean algebra.

Course objective

The course aims at providing fundamental concepts, effective problem-solving techniques, and the appropriate exposure to modern technologies, design techniques, and applications in the area of complex yet reliable VLSI digital circuits and systems, both combinational and sequential.

Course-related learning outcomes

Knowledge:
Students know principles and adanced rules used to design complex digital circuits. They also know various arithmetic building blocks employed in computer arithmetic. They learn how to design large and complex digital systems with the help of computer-aided design (CAD) and design for test (DFT) tools.

Skills:
Students can design a combinational digital circuit using, as guiding criteria, hardware complexity, speed of the circuit, its power consumption, and heat dissipation. Students understand models representing synchronous and clockless finite state machines and can run their synthesis process, including state minimization, state coding, flip-flop-based implementation, and safety analysis. Can devise a method to detect and localize failures in digital designs; can also assess a possible impact such methods may have on a circuit security.

Social competences:
Students appreciate the practical significance of the systems developed in the course. They are aware of limitations of modern digital circuits. They are open for new applications of digital devices in technology, science, and social (daily) life. Can express their own opinions with respect to currently used solutions and technologies in design of contemporary digital systems.

Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:

Knowledge acquired during the lectures is verified by a written colloquium. It consists of 8 open problems graded differently. Skills acquired in the laboratory classes are verified on the basis of fulfilling tasks assigned in a class or a project. In both cases, a passing threshold of 50% of the possible points is adopted. The following grading scale is used: < 50% - 2.0; 50%-59% - 3.0; 60%-69% - 3.5; 70%-79% - 4.0; 80%-89% - 4.5; 90%-100% - 5.0.

Programme content

Advanced topics in automated synthesis of multilevel digital circuits. Computer arithmetic and related devices. RTL and architectural-level designs. Reliability of digital circuits and systems. Automatic test pattern generation. Design for testability. Hardware security.

Course topics

Lectures: Automated synthesis of multilevel combinational designs. Binary arithmetics, binary integers, floating point arithmetic, arithmetic devices: adders, multipliers (Booth algorithm) and dividers, floatingpoint adders, IEEE 845 standard. Register transfer level (RTL) synthesis. Behavioral synthesis (the architectural level). Detection and localization of faults in combinational circuits. Fault modeling. Automatic test pattern generation (ATPG), fault simulation. Testing of sequential circuits. Design for testability. IEEE 1149.1 standard. Logic built-in self-test (LBIST). Test compression. Testing 2.5D and 3D designs. Memory test. Hardware security - basic design rules.
Labs: Design of optimized multilevel circuits, design of basic arithmetic circuits (adders and multipliers). RTL synthesis, the use of CAD tools, test generation for simple combinational designs.

Teaching methods

Lectures: a multimedia presentation.
Laboratory classes: students design certain simple digital circuits by using CAD tools, such as Multisim.

Bibliography

Basic:
1. J. Kalisz, Podstawy elektroniki cyfrowej, wyd. 5, WKŁ, Warszawa 2007.
2. J. Biernat, Arytmetyka komputerów, PWN, Warszawa 1996.
3. M.M. Mano, C.R. Kime, Podstawy projektowania układów logicznych i komputerów, WNT, 2007.
4. G. De Micheli, Synteza i optymalizacja układów cyfrowych, WNT, 1998.
5. T. Łuba (red.), Synteza układów cyfrowych, Wydawnictwa Komunikacji i Łączności, 2003.

Additional:
1. J. Tyszer, G. Mrugalski, A. Pogiel, D. Czysz, Technika cyfrowa - zbiór zadań z rozwiązaniami, Wydawnictwo BTC 2016.
2. J.P. Hayes, Digital logic design, Addison-Wesley 1994.
3. P.K. Lala, Practical digital logic design and testing, Prentice Hall 1996.

4. M. Tehranipoor, C. Wang, Introduction to hardware security and trust, Springer 2012.
5. L.-T. Wang, C-.W. Wu, X. Wen, VLSI test principles and architectures, design for testability, Elsevier Inc. 2006.

Breakdown of average student's workload

	Hours	ECTS
Total workload	60	2,00
Classes requiring direct contact with the teacher	45	1,50
Student's own work (literature studies, preparation for laboratory classes/ tutorials, preparation for tests/exam, project preparation)	15	0,50